WHAT IS CLAIMED IS:

1. A method of digitizing signals in an input buffer of a dynamic random access memory (DRAM) device, comprising:

providing a plurality of buffer modules, wherein each buffer module comprises a differential amplifier having a first input to receive a signal to be digitized and a second input to receive a reference voltage, a common source stage, and an output stage;

applying a bias voltage to control impedance of the common source stage; and

applying the reference voltage to define the amplitude of the bias voltage.

2. The method of claim 1 wherein the common source stage is connected between a common node of the differential amplifier and a ground reference of the buffer module and comprises an input responsive to the bias voltage.

3. The method of claim 2 wherein the common source stage is a field effect transistor having a first terminal coupled to a common node of the differential amplifier, a second terminal coupled to a ground reference of the differential amplifier, and a gate terminal responsive to the bias voltage.

4. The method of claim 1 wherein an output of the differential amplifier is coupled to an input of the output stage.

5. The method of claim 1 wherein an output voltage of the output stage asserts one of a logic high level and a logic low level.

6. The method of claim 1 wherein the source of a bias voltage comprises one of a controlled voltage-to-current converter and a controlled voltage-to-voltage converter.

7. The method of claim 1 further comprising:

increasing the bias voltage when the reference voltage increases; and

decreasing the bias voltage when the reference voltage decreases.

8. The method of claim 1 wherein timing and duration of the signal and the reference voltage are defined by a memory controller of the DRAM device.

9. A circuit configuration for an input buffer of signals in a dynamic random access memory (DRAM) device, comprising:

a plurality of buffer modules, wherein each buffer module comprises a differential amplifier having a first input responsive to a signal and a second input responsive to a reference voltage, a common source stage, and an output stage; and

a source of a bias voltage to control impedance of the common source stage, wherein the reference voltage defines the amplitude of the bias voltage.

10. The circuit configuration of claim 9 wherein the common source stage is connected between a common node of the differential amplifier and a ground reference of the buffer module and comprises an input responsive to the bias voltage.

11. The circuit configuration of claim 10 wherein the common source stage is a field effect transistor having a first terminal coupled to a common node of the differential amplifier, a second terminal coupled to a ground reference of the differential amplifier, and a gate terminal responsive to the bias voltage.

12. The circuit configuration of claim 11 wherein an output of the differential amplifier is coupled to an input of the output stage.

13. The circuit configuration of claim 9 wherein an output voltage of the output stage asserts one of a logic high level and a logic low level.

14. The circuit configuration of claim 9 wherein the source of a bias voltage comprises one of a controlled voltage-to-current converter and a controlled voltage-to-voltage converter.

15. The circuit configuration of claim 9 wherein the source of the bias voltage is configured to:

increase the bias voltage when the reference voltage increases; and

decrease the bias voltage when the reference voltage decreases.

16. The circuit configuration of claim 9 wherein timing and duration of the signals and the reference voltage are defined by a memory controller of the DRAM device.

17. A control system of a dynamic random access memory (DRAM) device, comprising:

a memory controller;

a plurality of lines propagating signals selected from at least one of data and control signals; and

an input buffer coupled to the plurality of the lines, the input buffer comprising:

a plurality of buffer modules for the signals, each buffer module comprising a differential amplifier having a first input responsive to an input signal selected from one of data and control signals and a second input responsive to a reference voltage, a common source stage, and an output stage; and

a source of a bias voltage to control impedance of the common source stage, wherein the amplitude of the bias voltage is controlled by the reference voltage.

18. The control system of claim 17 wherein the common source stage is a field effect transistor having a first terminal coupled to a common node of the differential amplifier, a second terminal coupled to a ground reference of the differential amplifier, and a gate terminal responsive to the bias voltage.

19. The control system of claim 17 wherein the source of the bias voltage is configured to:

increase the bias voltage when the reference voltage increases; and

decrease the bias voltage when the reference voltage decreases.

20. The control system of claim 17 wherein timing and duration of the at least one of data and control signals, the reference voltage, and the bias voltage are defined by the memory controller.

21. A dynamic random access memory (DRAM) device, comprising:

an array of DRAM memory cells;

a memory controller;

a source of signals selected from at least one of data and control signals;

a source of a reference voltage; and

at least one buffer module comprising:

a differential amplifier having a first input responsive to one of a data signal and a control signal and a second input responsive to the reference voltage, a common source stage, and an output stage; and

a source of a bias voltage to control impedance of the common source stage, wherein a reference voltage defines the amplitude of the bias voltage.

22. The DRAM device of claim 21 wherein the source of the bias voltage is configured to:

increase the bias voltage when the reference voltage increases; and

decrease the bias voltage when the reference voltage decreases.

23. The DRAM device of claim 21 wherein an output voltage of the output stage asserts one of a logic high level and a logic low level.

24. The DRAM device of claim 21 wherein timing and duration of the at least one of data and control signals, the reference voltage, and the bias voltage are defined by the memory controller.

25. A circuit configuration for an input buffer of a signal, comprising:

a differential amplifier having a first input responsive to the signal and a second input responsive to a reference voltage;

a common source stage connected between a common node and a ground reference of the differential amplifier;

an output stage coupled to an output of the differential amplifier; and

a source of a bias voltage to control impedance of the common source stage, wherein the reference voltage defines the amplitude of the bias voltage.

26. The circuit configuration of claim 25 wherein the common source stage is a field effect transistor having a first terminal coupled to the common node of the differential amplifier, a second terminal coupled to a ground reference of the differential amplifier, and a gate terminal responsive to the bias voltage.

27. The circuit configuration of claim 25 wherein the source of the bias voltage is configured to:

increase the bias voltage when the reference voltage increases; and

decrease the bias voltage when the reference voltage decreases.

28. The circuit configuration of claim 25 wherein an output voltage of the output stage asserts one of a logic high level and a logic low level.

29. A method of digitizing a signal, comprising:

providing an input buffer comprising:

a differential amplifier having a first input responsive to the signal and a

second input responsive to a reference voltage;

a common source stage connected between a common node and a ground reference of the differential amplifier and comprising an input for a bias voltage; and

an output stage coupled to an output of the differential amplifier; and controlling impedance of the common source stage in response to receiving the bias voltage on the input of the common source stage; and

defining the amplitude of the bias voltage in response to receiving the reference voltage on the second input of the differential amplifier.

30. The method of claim 29 wherein the common source stage is a field effect transistor having a first terminal coupled to a common node of the differential amplifier, a second terminal coupled to a ground reference of the differential amplifier, and a gate terminal responsive to the bias voltage.

31. The method of claim 29 wherein the bias voltage is provided by a bias voltage source configured for:

increasing the bias voltage when the reference voltage increases; and

decreasing the bias voltage when the reference voltage decreases.

32. The method of claim 29 wherein an output voltage of the output stage asserts one of a logic high level and a logic low level.